A high speed dual modulus divider in SOI CMOS with stacked current steering phase selection architecture.

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Abstract — **This work describes a high frequency dual modulus divider designed and fabricated in a 0.35μm PDSOI process, employing a stacked topology phase switching scheme. SOI CMOS technology is exploited to allow current re-use in a higher supply voltage than dictated by single device breakdown. Measurements show the circuit operating at 3GHz (Vdd=6.8V.)**

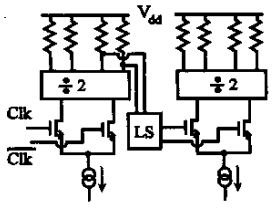
I. Introduction

Integrated wireless transceiver ICs often employ one or more frequency synthesisers as part of a complete radio system, and they are often required to run at frequencies well above that of the RF signal. Applications such as wireless LAN, GPS and cellular radio have demanded the use of advanced silicon and SiGe process technologies to allow the realisation of practical architectures [1]. However, particularly in the case of bulk CMOS technology, the gain in speed resulting from a smaller feature size has come at the expense of lower on-chip supply voltage. This can be a problem for analogue and RF designers, as it restricts the number of stacked transistors and can degrade the performance of a circuit.

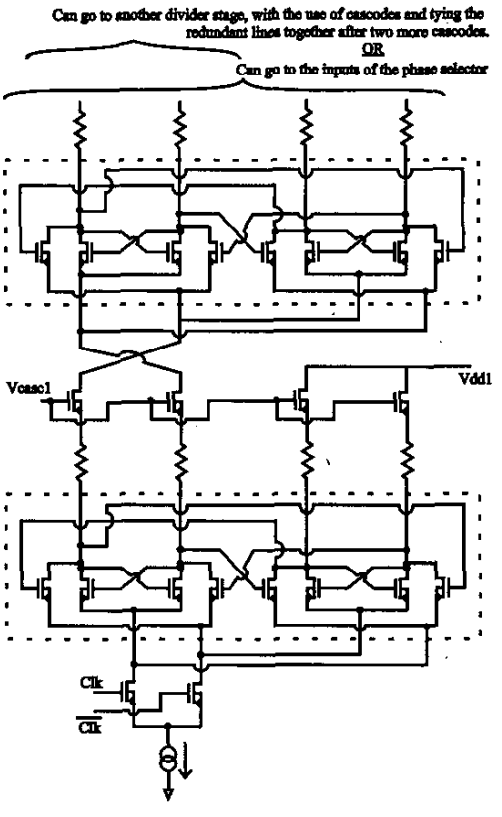
This work presents a dual modulus divider implemented in SOI CMOS and is intended for multi-GHz synthesiser applications. In addition to benefiting from the lower parasitic capacitances of SOI, the technology is further exploited by stacking several circuit blocks on a single supply current branch. Complete device isolation allows the total supply voltage to exceed the rating of each individual device without major risk of gate oxide breakdown.

II. Silicon on Insulator

The work described in this paper is based on partially depleted SOI CMOS technology, using both floating-body and body-tied structures [2]. These are thick film devices that have drain and source implants extending to the back oxide, electrically isolating their body regions (unlike bulk CMOS designs that have a common body connection). Without an explicit body contact, the device is said to have a 'floating body', and at low frequencies, its drain current shows the characteristic 'kink' in its behaviour. Tying the body region to a fixed relative potential (usually the source) using



(a) Voltage mode cascading.



(b) Stacking with current mode cascading.

Fig. 1. Diagrams showing methods available in SOI design, for cascading divide by 2 stages asynchronously.

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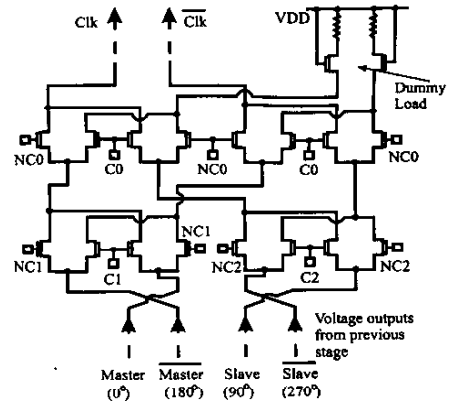
an ohmic tap largely eliminates this behaviour, by allowing charge to flow freely in and out of the body region. Unfortunately, in high density designs, adding such taps consumes area, adds parasitic capacitance and reduces packing density.

With source/drain implants reaching the back oxide, the depletion capacitances associated with the source/drain terminals are greatly reduced, and this has caught the attention of many design groups. This back oxide also exascerbates self-heating effects; the inability to dissipate heat can cause DC characteristics to change, though the thermal gradient is not normally severe for high speed switching devices. For successful designs, accurate, robust compact models are required. In this work we have used the STAG model [3] which takes into account both self-heating and floating body effects.

III. Divider Design

A. Divide by 2

Conventional divider designs use source coupled logic (SCL) to construct latches, often with source followers between stages for level shifting and buffering. As in most high speed MOS logic, the back bias on upper transistors in the stack of devices becomes significant, reducing headroom and slowing the circuit [2]. In our designs, the SOI dividers have transistor bodies tied to their own source terminals, with the obvious benefit that the back gate effect is eliminated and circuit speeds are improved. Note that body ties have not been used in the first two divider stages (resulting in floating body devices) as simulations showed the maximum speed of the divider stack increasing to 6.5GHz before layout; this is due to the reduced predicted capacitive loading of the drain-body reverse diode. The ability to stack devices has been taken a step further by stacking several complete circuit blocks [4]. Several divider blocks are arranged in series mode with high frequency inputs arriving as currents superposed on the supply current at the bottom of the stack (NMOS based divide by 2 stages). Figure 1 shows the different approaches of voltage- and current-mode cascading. With the latter, it is apparent that the need for level shifting is largely removed, which is beneficial as it would either require capacitive coupling (giving problems at high frequencies owing to parasitic capacitance to ground), or a source follower (introduces phase shift and doesn't act differentially, as well as consuming more current). Furthermore, stages taking their outputs from the early stages in the division chain will require less bias current due to their slower operating frequency, and hence part of the fast cell current can be re-used in other associated circuit functions. At each stage, the individual cells operate with a supply voltage drop well within the device breakdown limits, avoiding stress to any individual device gate oxide.



(a) Schematic of the phase selector.

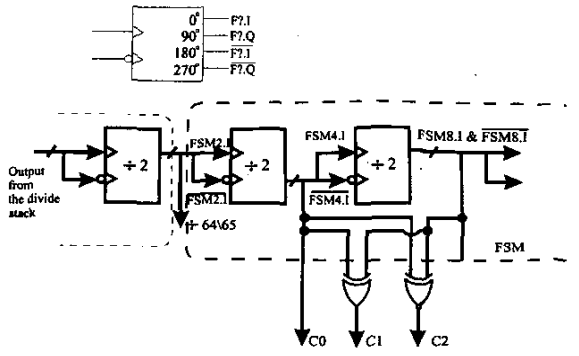
$C2$	$\overline{C2}$	$C1$	$\overline{C1}$	$C0$	$\overline{C0}$	Output .
1	0	0	1	0	1	$B{\cdot}I$ (S0)
0	1	0	1	0	1	$B{\cdot}I$ (S1)
0	1	0	1	1	0	$B{\cdot}Q$ (S2)
0	1	1	0	1	0	$B{\cdot}Q$ (S3)
0	1	1	0	0	1	$\overline{B{\cdot}I}$ (S4)
1	0	1	0	0	1	$\overline{B{\cdot}I}$ (S5)
1	0	1	0	1	0	$\overline{B{\cdot}Q}$ (S6)
1	0	0	1	1	0	$\overline{B{\cdot}Q}$ (S7)

(b) Table showing the input combinations for the 4 phases.

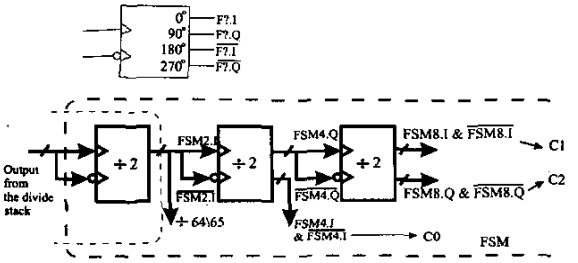
Fig. 2. Phase selecting implementation, the core of the dual modulus function.

B. Phase Selecting

Dual modulus division is accomplished using a phase selection concept [5]. In this design, the phase selection is implemented using a 4 to 1 current steering channel selector as shown in figure 2, which has the advantage that it too can be stacked on top of the divider stages. The selector can be controlled using signals from a 4-state finite state machine (FSM) at the output of the divider stack (figure 3(a)). However this leads to glitches in the output when changing from phase to phase, ie, between states S0, S3, S4 and S7 (shown in the table of figure 2(b)). By using a Gray code style sequencing, and an input to an 8-state FSM at twice the original frequency, these glitches are removed by using all 8 states (figure 3(b)). This does not pose any overhead on the layout as the last divide stage of the 64/65 divider is included in the 3-bit FSM. An additional benefit is that the XOR gates are eliminated by chosing different quadratures of the SCL-based divide stages within the FSM.



(a) Logic implementation for the FSM where only 4 states are present.



(b) Logic implementation for the employed FSM with 8 states.

Fig. 3. Diagrams showing two possibe structures for the state machine.

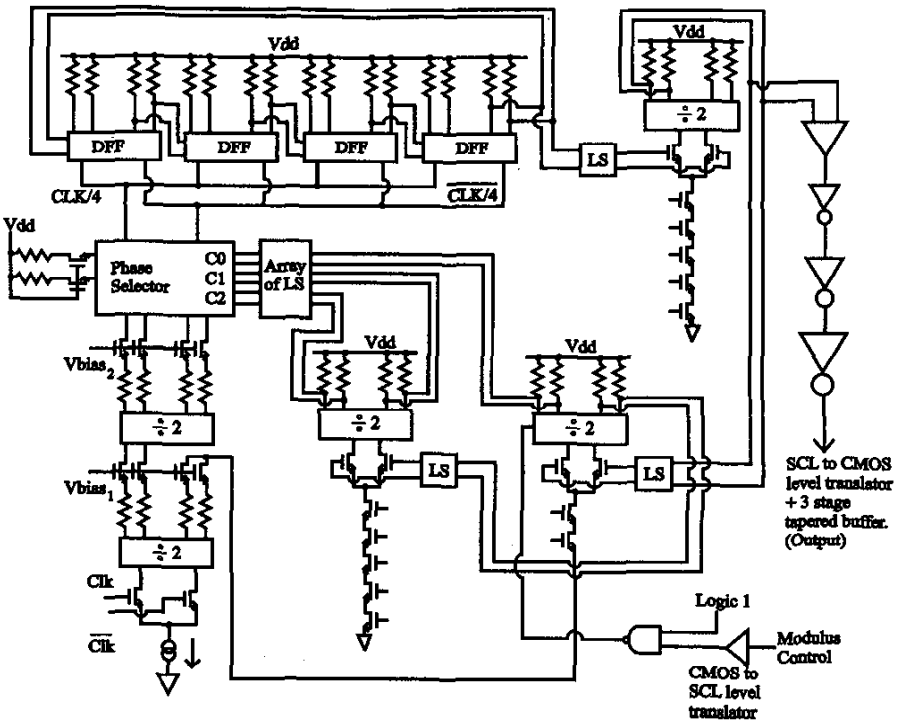
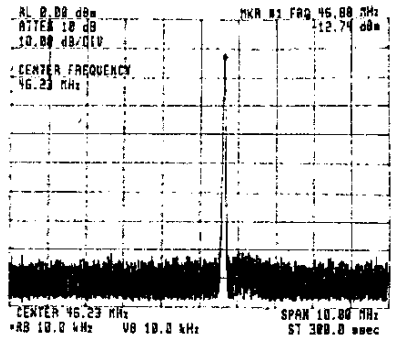


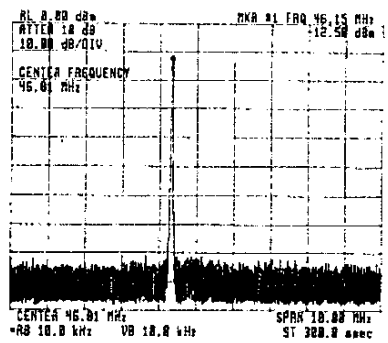
Fig. 4. Schematic of the full dual modulus divider.

C. Full Divider

A schematic of the whole divider is shown in figure 4. Two high-speed asynchronous dividers precede the phase selector, enabling the swallowing of an input clock pulse. As the divide by 2 stages are stacked, the total current through each is halved and this binary reduction leads to slower output transitions. Simulations show that capping the stack with a synchronous divide by 8 can restore the edges(constructed from 4 D-type flip-flops (DFF)). The total division of the stack is 32. Another divide by 2 is placed off the stack giving ratios of 64 and 65. This off-stack divider, together with two more off-stack dividers, generate the 8 states of the FSM. To limit the local power sup-



ide by 64.



(b) Divide by 65.

Fig. 5. Plots showing the output after dividing a 3GHz input.

ply seen, these divide by 2 units have to be supported by cascodes. Through an additional current reuse branch, the second off-stack divider sinks its current into the redundant output of the first stage of the stack. A point regarding the off-stack dividers is that source followers are required to cascade the divide stages. The gate voltages for these cascodes are generated by an on-chip bias network, and this is driven by the same reference current source used to drive the divider. The modulus control has been implemented through the use of a NAND gate embedded in the second off-stack divider. A CMOS-to-SCL translator is included to control the modulus, whilst a three stage tapered buffer is included to give a lower frequency CMOS rail-to-rail output. Each high frequency input has a 50 Ohm on-chip termination to ground, and the common mode voltage is set internally using diode-connected nMOS transistors.

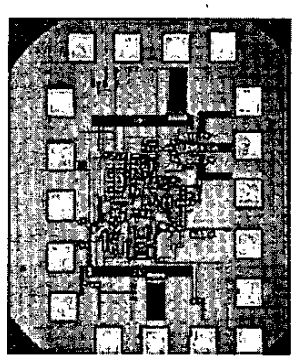


Fig. 6. Photo of divider die.

IV. Measurements

Figure 5 shows the output waveforms/spurs of the dual modulus divider. A sawn die (figure 6) was mounted on an alumina substrate and wire-bonded to gold conductors. 50 Ohm matched microstrips connect the signal source to the die (also includes a hybrid in the test setup to generate the differential signal). The current consumption is 10mA with a 6.8V power supply. With a 3GHz input (233mVpp) around a 1.8V common-mode voltage, the output is a 2.5V square wave running at 46.875MHz and 46.154MHz for division by 64 and 65 respectively. The size of the design including pads is 1.5mm by 1.4mm.

V. Conclusion

A 64/65 dual modulus divider has been reported using stacked cells for current re-use in the divider chain and phase selector. An efficient current steering topology for selecting signal phases has been illustrated together with a description of the FSM controlling it. The 0.35μm PDSOI fabricated chip runs with a maximum input frequency of 3GHz drawing 10mA from a 6.8V power supply.

Acknowledgement

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References

[1] David Su, et. al.,"A 5GHz CMOS transceiver for IEEE802.11a wireless LAN," *ISSCC Digest of Technical Papers*, Paper 5.4, Feb. 2002.

[2] W.Redman-White and K.Bernstein, "SOI CMOS CIRCUIT DESIGN EXPOSED - ANOTHER DIRTY TRICKS CAMPAIGN?," Invited Paper, *Proceedings of ESSCIRC 2000*, Stockholm, Sept 2000.

[3] M.S.Lee, et. al., "A physically based compact model of partially depleted SOI MOSFETs for analog circuit simulation", *IEEE J. Solid-State Circuits*, vol. 36, pp.110-121, Jan 2001.

[4] K.Mistry, et. al., "Low power multi-gigahertz divider architectures in SOI CMOS employing series current reuse," *Proceedings of the European Conference on Circuit Theory and Design*, Helsinki, August 2001.

[5] J.Craninckx and M.Steyaert, "A 1.75GHz/3V dual modulus divide-by-128/129 prescaler in 0.7μm CMOS," *IEEE J.Solid-State Circuits*, vol.31, pp.890–897, Jul 1996.